Studies on Sensitivity of Clock and Data Recovery Circuits to Power Supply Noise

Khalil I. Mahmoud, J. Dhurga Devi, R. Rajasekar, and P. V. Ramakrishna

Abstract—This paper deals with the study of the impact of power supply noise on the performance of CMOS Clock and Data Recovery (CDR) Circuits. The sensitivity of the various blocks of the dual loop CDR circuit to power supply noise is first studied and then it is demonstrated that incorporation of suitable Low Dropout Regulators (LDOs) can enhance the performance of the CDR system with respect to power supply noise. Based on extensive simulations, it was observed that while the system can tolerate only about 20mV/10MHz noise on the power supply, incorporation of LDOs enables it to tolerate 200mV/10MHz noise without degradation in performance.

Index Terms—CDR, PLL, VCO, jitter, power supply noise.

I. INTRODUCTION

Clock and Data Recovery (CDR) circuits have been continuously evolving over the past few decades, with the requirements for ever increasing data rates, lower supply voltages and scaling of technology. These CDR circuits cater to multiple standards like SATA, PCI Express, XAU, OC-192 and so on. Different CDR circuits are expected to be optimized for operation at frequencies that could be anywhere between 1GHz and 100GHz for application over distances varying from about a few centimeters to about a few 100 meters.

The literature on CDR circuits is vast and the architectures have been continuously evolving over the past two decades. The crucial role played by the CDR circuits can be gauged from the number of recent tutorial and review articles [1]-[4] published on this topic. The literature cited in [1]-[4] largely deal with techniques to increase the speed of operation (data rates), techniques for the mitigation of ISI, tradeoffs between jitter, loop bandwidth, tunability, area, power consumption and so on. There are only a few important architectures widely used for implementing CDR systems, and amongst these, the dual loop CDR architecture [5] is considered as an important one [1], [6]. Being analog in nature, with independent loop filters for frequency lock loop and the phase locked loops, it enables one to achieve a wide operating frequency range while maintaining low jitter.

For CDR systems, very few quantitative studies have been reported on the impact of power supply noise on the performance. The CDR systems are closely related to Phase Locked Loop (PLL) and both share a number of similar characteristics, including the impact of power supply noise. Even for PLLs, which cater to a much wider range of applications, studies on the mitigation of power supply noise have been reported only recently in [7], [8]. A method to minimize the supply sensitivity of a CMOS ring oscillator through joint biasing of the supply and the control voltage is proposed in [9] for PLLs. The work presented in [10] proposes adding a current source in parallel with PMOS transistor of the inverter to form a pseudo-differential ring oscillator. The current source provides a large impedance between the output node and the supply, effectively isolating these two nodes and making the oscillator frequency less sensitive to supply voltage changes. An architecture to decouple the tradeoffs between supply noise rejection and power consumption by putting the regulator outside the main loop of the PLL has recently been proposed in [11]. The decoupling is achieved by putting the regulator in the low bandwidth coarse loop, which allows maximizing the bandwidth to suppress the oscillator phase noise without affecting the power supply-noise rejection or the power dissipation of the regulator. In the context of CDRs, the emergence of power supply noise as a design constraint is emphasized in [2], and a procedure for carrying out fast simulations to evaluate the impact of power supply noise on CDR systems has been presented recently in [12]. The present work adds to this literature, and reports, for a specific CDR architecture, the studies carried out on the impact and mitigation of power supply noise.

In the context of CDRs, the emergence of power supply noise as a design constraint is emphasized in [2], and a procedure for carrying out fast simulations to evaluate the impact of power supply noise on CDR systems has been presented recently in [12]. The present work adds to this literature, and reports, for a specific CDR architecture, the studies carried out on the impact and mitigation of power supply noise.

The present paper is organized as follows. In Section II, presents the details of the design of the dual loop delay interpolating CDR system. In Section III, the design of the LDO circuits is presented. In Section IV, the simulations results have been presented and discussed. Section V presents the conclusions.

II. THE DUAL LOOP CDR SYSTEM DESIGN

The dual loop delay interpolating CDR architecture chosen for the present study and adapted from [5], is shown in Fig.1 in the form of a block diagram. This system is considered as a reference for the present work and for which the jitter performance will be investigated. The system shown in Fig.1 consists of a coarse Frequency Lock Loop (FLL) and a fine Phase Lock Loop (PLL). The FLL consists of a Frequency Detector (FD), Charge Pump (CP), Loop Filter (LPF) and a

All authors are with the Department of Electronic and Communications Engineering, Anna University, Chennai, Tamil Nadu, 600025, India. E-mail: khalilaljabory@gmail.com.
Voltage Controlled Oscillator (VCO). The FD is realized using a digital quadricorrelator which generates a number of constant duration UP and DOWN pulses proportional to the frequency difference between the data and an internally generated clock signal from the VCO. These UP and DOWN pulses control a charge pump output current that charges or discharges a loop filter. A second order loop filter is used for the FLL. The voltage developed at the output of the loop filter is corrected to the required common mode voltage by a Common Mode Feed Back (CMFB) circuit and then fed as coarse control voltage to the VCO. The VCO is common to FLL and PLL loops.

The VCO used in this work is the same as that of [13] and consists of a ring oscillator with four delay interpolator stages. It also has two differential control voltages, one coarse voltage (Vcoarse) from the FLL and one fine voltage (Vfine) from the PLL. These control voltages are used to steer the tail currents of the delay interpolating stage in the fast path and in the slow path. The fast and slow path have different current magnitudes, but always their sum remains the same.

A single delay interpolator stage of the ring oscillator is shown in Fig.3 with a slow path comprising of a constant delay buffer stage followed by another inverter delay stage, while the fast path has only one inverting delay stage. The currents \(I_{fast,o}\) and \(I_{slow,o}\) are derived from current folding circuit controlled by the differential control voltage of the PLL, while the \(I_{slow,in}\) and \(I_{fast,in}\) currents are derived from current folding circuit controlled by the differential voltages of the PLL. The ring oscillator VCO is designed with four such delay interpolating stages. The VCO generates the in-phase and the quadrature phase clock, which is required for the FD in the PLL, while the in-phase and out of phase clock are required for the PD in the PLL. When the frequency locks, the variation on the coarse control voltage becomes insignificant and the VCO is controlled only by the PLL [5].

The design procedure and relevant equations for determining the loop parameters can be obtained by adopting the procedure given in [5] and [14]. For a nominal data rate of 1.075Gbps chosen for the CDR, the FLL cross over frequency \(\omega_c\) is chosen as 207Mrad/s, the VCO sensitivity is selected as 1.58GHz/V. The charge pump current of the FLL is found to be 125uA. The devices chosen for the simulations are from 0.35um CMOS technology libraries from Austriamicrosystems. The design equations used for determining the loop filter parameters are summarized below.

\[
\omega_c = \frac{I_{cp} \cdot K_{VCO} \cdot R_p}{2 \cdot \pi}\quad (1)
\]

\[
\omega_z = \frac{\omega_c}{5} = \frac{2 \cdot \pi \cdot R_p \cdot C_p}{1}\quad (2)
\]

\[
\omega_p = 5 \cdot \omega_c = \frac{C_p + C_s}{C_p \cdot C_s \cdot R_p}\quad (3)
\]

\[
C_s = \left[\frac{\omega_p \cdot R_p - \frac{1}{C_p}}{\pi}\right]^{-1}\quad (4)
\]

The symbols \(\omega_c\), \(\omega_p\), \(\omega_z\), \(\zeta\), and \(K_{VCO}\) are the crossover frequency, pole frequency, zero frequency, damping ratio, and VCO gain respectively, while \(R_p\), \(C_p\), and \(C_s\), represent the shunt resistor, capacitor and parallel smoothing capacitor respectively of the FLL loop filter. Using the above design equations and system specifications, the parameters of the second order loop filter for FLL have been determined and are listed in Table 1.

The PLL consists of an analog Phase Detector (PD), V-to-I converter, Low Pass Filter (LPF) and the VCO [5]. The PD in the PLL is a differential analog sample and hold circuit which holds the clock amplitude on a capacitor for each data transition. The V-to-I converter block is necessary for converting the differential PD output linearly to a current that charges or discharges the loop filter capacitor (which is a simple lead-lag filter) to provide a voltage. The control voltage is then corrected by the CMFB circuit to the required common mode level.

The PLL loop natural frequency \(\omega_n\) and damping ratio \(\zeta\) are chosen to be 3Mrad/s and 4 respectively and the VCO sensitivity (fine) is 198MHz/V for the fine control voltage. The design procedure for determining the PLL loop filter parameters is adopted from [14] and the design equations are as follows:

\[
\tau_2 = \frac{2 \cdot \zeta \cdot \omega_n}{\pi}\quad (5)
\]

\[
K = K_{pd} \cdot K_{VCO} \cdot \frac{\pi}{4}\quad (6)
\]

\[
K = 2 \cdot \zeta \cdot \omega_n \cdot \sqrt{\frac{\tau_1}{\tau_2}} + 1\quad (7)
\]
The symbols $\omega_n$, $\zeta$, $K$, $K_{pd}$, and $K_{VCO}$ are the natural frequency, damping ratio, open loop gain, phase detector gain, and VCO gain respectively. The symbols $\tau_1$, $\tau_2$, $R_{f1}$, $R_{f2}$, and $C$ represent the time constants, series resistor, shunt resistor and capacitor respectively of the PLL loop filter. With these design equations and system specifications, the Lead-Lag loop filter parameters for PLL are determined and tabulated in Table 1.

**TABLE I**

<table>
<thead>
<tr>
<th>PLL LPF Parameter</th>
<th>Value</th>
<th>FLL LPF Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_1$</td>
<td>106.7k</td>
<td>$R_1$</td>
<td>1.05k</td>
</tr>
<tr>
<td>$C_p$</td>
<td>28.8pF</td>
<td>$R_2$</td>
<td>835k</td>
</tr>
<tr>
<td>$C_s$</td>
<td>7.2pF</td>
<td>$C$</td>
<td>150pF</td>
</tr>
</tbody>
</table>

For the above CDR design, detailed simulations were carried out to verify its operation first and then various simulations were carried out with respect to its power supply noise immunity. The results obtained are presented in subsequently in section IV.

In order to improve the power supply noise immunity of the above CDR, suitable LDO circuits have been designed and these are discussed in the next section.

### III. THE PROPOSED LDO DESIGN

The CDR system with two LDOs connected between the power supply and the dual loop delay interpolating CDR system blocks is shown in Fig.3. Two LDOs are used to satisfy the different requirements of the CDR system since the FD and PD operates at low frequency and consumes high transient currents, while the rest of CDR system operates at high frequency and low currents. One LDO is therefore connected to FD and PD, while the other required is connected to the rest of CDR system.

In the split-regulator architecture for LDOs suggested in [15], due to a distribution of load currents across the different LDOs, the sizes of the pass devices can be reduced. This makes the output pole of the regulator as the dominant pole rather than amplifier pole, and this in turn leads to an increase in the Power Supply Rejection (PSR) at high frequencies. The present paper uses the Miller compensated regulator with an additional NMOS cascode device as suggested in [16] along with the split-regulator architecture to feed power to the entire CDR system. The decrease in pass transistor size is used to reduce the load capacitance required rather than to change the location of poles. The required PSR is now enhanced by NMOS cascode device.

The architecture of LDO used is shown in Fig.4 and it is the same as that discussed in [16]. A single stage CMOS OTA is used as an error amplifier. The PMOS transistor MP is used as a pass device where as the NMOS device M1 is used as a cascode device. The charge pump is used to boost the gate voltage $V_{ch}$ of NMOS cascode device beyond VDD, while an RC filter (not shown) is used to reduce high frequency noise from the charge pump. The regulated output voltage is $V_{sup} = 3.0V$ from an input VDD = 3.6V supply. The dropout of the cascode NMOS is 250mV and that of PMOS pass device is 350mV. These results are verified through simulations. Further, a 10MHz a 200mVp−p sinusoidal signal at the input power supply of the LDO gave a ripple of 5mVp−p signal at the regulated output terminal.

IV. RESULTS AND DISCUSSION

First, simulations were carried out with a clean power supply so that this can be treated as a reference against which the noisy case can be compared. Next, noise in the form of sinusoidal signal was added to the power supply of the CDR system to test the capability of the CDR system to tolerate power supply noise. Jitter was then measured from the recovered clock for various applied noise amplitudes. The maximum supply noise amplitude that can be tolerated by the CDR system was determined by observing the failure of the system to lock as the supply noise amplitude was increased. The individual blocks of the system were separately tested with this maximum supply noise amplitude that can be tolerated. The most sensitive block of the system was then identified by measuring the jitter from the recovered clock. Finally, the CDR system with the two LDOs was subjected to...
similar noise and maximum power supply noise that can be tolerated by the system was observed.

Using a clean 3.0V power supply, the control voltages generated by the FLL and the PLL for the nominal case are shown in Fig.5. It can be seen that the CDR establishes lock after about 600ns for the FLL and after 700ns for the PLL. These and the subsequent transient responses have been obtained with $2^{14}$ Pseudo Random Bit Stream (PRBS) data as input.

In order to determine its ability to tolerate power supply noise, this CDR system was then simulated with a noisy power supply common to the whole CDR. The noise applied on the power supply was a sine wave with 10MHz and variable amplitudes from 10mV to 30mV were applied. The resulting output jitter on the recovered clock and the ripple on control voltages were measured.

For 10mV and 20mV noise amplitudes, the dual loop delay interpolating CDR system captured the frequency and phase correctly. From Fig.6 and Fig.7, it can be seen that the ripple on the differential control voltage is within reasonable limits. The measured jitter on the recovered clock is given in Table II, but will be discussed subsequently along with the LDO case. When the noise amplitude was increased to 30mV the resulting control voltage is plotted and shown in Fig.8. Though not evident in Fig.8, for this case, lock was not established. Actually it was found that clock recovery fails when supply noise is more than 20mV amplitude at 10MHz, the differential control voltage does not settle down but continues to oscillate.

Fig. 7. The fine control voltage of the CDR system with 20mV/10MHz noise on power supply.

Next, in order to determine the particular block within the CDR which is most sensitive to power supply noise, the following procedure is adopted. The noise on the power supply is applied, one at a time, on each individual block of the CDR and the ripple on control voltage and the jitter on the recovered clock are measured. As already pointed out, 20mV/10MHz is the maximum noise that can be tolerated by the whole system without LDO, and this noise level is applied to each block separately while the rest of the blocks were fed with clean supply.

In the present architecture, the FD is basically a digital architecture and hence less sensitive to power supply noise. Fig.9 shows plots of the differential fine control voltage with noise injected selectively at the FD power supply node, while the other nodes were fed with clean supply. Similarly, the PD is not susceptible to supply noise because it can get rejected by the loop filter if it is outside the pass band. Fig.10 shows plots of the differential fine control voltage with noise injected selectively at PD power supply node, while the other nodes were fed with clean supply. Next, the VCO is a quite susceptible to noise on the VCO supply line. The noise on the VCO supply disturbs the clock frequency and is not necessarily rejected by the loop filter. The noisy power supply is applied only to the VCO. Fig.11 show the differential fine
control voltage which has the largest ripple on the control voltage and proves that the VCO is the most sensitive part of the CDR system to power supply noise. Fig.9, Fig.10, and Fig.11 are then superposed on the same plot and shown in Fig.12 to show a comparison between the differential control voltages (fine) for the three cases considered and it is clear that VCO gives rise to the largest ripple on the control voltage. The corresponding jitter on recovered clock is also measured and is found to be 37.39ps, 17.55ps, and 5.82ps when noise is injected into the VCO, PD, and FD supply nodes respectively.

As described in the previous section, inclusion of LDOs in the supply lines of the CDR is expected to improve the performance of the system with respect to power supply noise. Even though the FD and PD are not vulnerable to high frequency noise on the supply line, they are sensitive to supply noise that falls within the pass band of the loop filter. Hence one LDO is inserted into the supply line feeding the VCO and another LDO is inserted into the supply lines feeding the rest of the system.

The inputs to both the LDOs are provided with noisy power supply of varying amplitudes and the resulting jitter on the recovered clock from the CDR were determined. With the LDOs in place, Fig.13 shows that the CDR system can operate without significant degradation even when the power supply noise of 200mV at 10MHz is injected into the power supply line. Fig.13 should be contrasted with Fig.11 which is for the case when only 20mV/10MHz noise applied to VCO alone but without any LDOs.

The jitter on recovered clock and ripple on the differential fine control voltage of the PLL is shown in Table II. It can be seen that the jitter for the case of noise of 200mV/10MHz with LDO is less than the jitter for a noise of 20mV/10MHz without LDO. The ripples on differential fine control voltages for noise amplitudes of 50mV, 100mV, and 200mV with the LDO case are nearly one third of corresponding values for the case without LDO.

In conclusion, the dual loop delay interpolating CDR with LDOs can tolerate noise of the order of 200mV/10MHz while the dual loop delay interpolating CDR without LDOs can...
hardly tolerate more than 20mV/10MHz before losing lock.

<table>
<thead>
<tr>
<th>TABLE II</th>
<th>THE CDR PERFORMANCE WITH AND WITHOUT LDOs (N.L.: NOT LOCKED)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Without LDO</td>
</tr>
<tr>
<td>Noise Amplitude</td>
<td>10mV</td>
</tr>
<tr>
<td>Jitter</td>
<td>16.4ps</td>
</tr>
<tr>
<td>Ripple</td>
<td>60mV</td>
</tr>
</tbody>
</table>

V. CONCLUSIONS

In conclusion, the present study indicates that (a) the dual loop CDR architecture is vulnerable to supply noise in the range of 10-20mV and (b) the incorporation of separate and appropriately designed LDOs can make the entire system to operate without significant degradation even for supply noise of the order of 200mV up to 10MHz frequencies.

ACKNOWLEDGMENT

The author would like to thank Iraq-India governments for their financial support of the Scholarship through Indian Counsel for Cultural Relations (ICCR).

REFERENCES


Khalil I. Mahmoud is a PhD student at ECE Dept., CEG Campus, Anna University, Guindy, Chennai-25, India.

J. Dhurga Devi is a PhD student, and Lecturer at ECE Dept., CEG Campus, Anna University, Guindy, Chennai-25, India.

R. Rajasekar is a M.Sc. student at ECE Dept., CEG Campus, Anna University, Guindy, Chennai-25, India.

P. V. Ramakrishna is a Professor at ECE Dept., CEG Campus, Anna University, Guindy, Chennai-25, India.