Transistor Aging Prediction in Nanometer Digital Circuits

Kyung Ki Kim

Abstract—In nanometer technology, accurate aging prediction of MOSFET digital circuits is one of the most critical issues for more reliable adaptive system design. This paper proposes a new on-chip aging prediction circuit to monitor BTI and HCI aging effects on digital circuits. The proposed circuit deploys a flip-flop based delay detector for monitoring a guardband violation of sequential logics. The outputs of the proposed circuit can be used as a control signal in reliable self-adaptive systems. A 0.11 µm CMOS technology has been used to implement and evaluate the proposed circuits.

Index Terms—Aging effect, aging prediction, bias temperature instability, hot carrier injection, reliability.

I. INTRODUCTION

As technology is scaled down more aggressively, it has become ever harder to design reliable circuits with each technology node. Under normal operation conditions, a transistor device can be changed by various stress sources such as negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), hot carrier injection (HCI), and time-dependent dielectric breakdown (TDDDB). The NBTI has become a key reliability issue in nanometer PMOS devices. It describes the parameter degradation under a negative (static) bias stress mode at elevated temperature. A corresponding dual effect, known as PBTI, is seen for NMOS devices, when a positive (static) bias stress is applied across the gate oxide of the NMOS device [1]-[4]. The HCI causes a degradation of the electrical parameters of a transistor when the transistor is switching [5]-[8]. The TDDDB causes a conduction path to form through a gate dielectric layer placed under electrical stress, leading to parametric or functional failure [9][10]. These stress sources (NBTI, PBTI, HCI, and TDDDB) change the threshold voltage of the transistor device, which causes temporal degradation in device reliability and even result in failures in the transistor circuits.

The reliability (aging) effect has traditionally been the area of process engineers. However, in the future, even the smallest of variations can slow down a transistor’s switching speed, and an aging device may not perform adequately at a very low voltage. Because of such dilemmas, the transistor aging is emerging as a circuit designer’s problem. Therefore, circuit designers need to consider these reliability effects in the early stages of design to make sure there are enough margins for circuits to function correctly over their entire lifetime. However, such an approach excessively increases the size and power dissipation of a system. This challenge for resilient circuits will require a design paradigm shift in all aspects of VLSI design. As the impact of reliability, new techniques in designing aging-resilient circuits are necessary to reduce the impact of the aging stresses on performance, power, and yield or to predict the failure of a system.

As an easy solution to the aging phenomena, circuit designers need to consider these reliability mechanisms in the early design stages to make sure that MOSFET circuits are operated with enough margins (called guardband) to function correctly over their entire lifetime. However, since this solution excessively increases the circuit size and power dissipation of a system, new circuit design techniques should be introduced for the resilient circuits. This challenge for resilient circuits will require a design paradigm shift to adaptive design for overcoming the performance degradation due to aging phenomena; in addition, an accurate on-chip prediction circuit technique to monitor aging phenomena would be one of the key issues in the adaptive design techniques. The outputs of the prediction circuits can be used as control signals in the new self-adaptive system using effective methods such as adaptive body biasing, supply voltage scaling, frequency scaling, etc.

For a good adaptive technique, the self-adaptive system has to include an on-chip aging prediction circuits whose outputs are strongly correlated with threshold-voltage degradation caused by aging stresses. In this paper, we propose a new one-chip aging prediction circuit which detects a guardband violation of sequential logics. Recently, on-chip NBTTI sensor circuits have been proposed, but they have some weak points in measuring the impact of NBTTI on digital circuits: Ref. [11] and [12] proposed a fully digital on-chip NBTTI monitor, but the proposed circuits suffer from a less direct correlation between the frequency-degradation of the monitor circuit and the $V_t$-degradation caused by NBTTI stress. Ref. [13] presents a compact structure in the sub-threshold region to digitalize the NBTTI stress, but the presented structure is too sensitive to temperature variation due to the circuit operation in the sub-threshold region. Ref. [14] proposed a circuit aging failure prediction scheme using the detection of a guardband violation, but the scheme has a complicated delay element with large area overhead. Moreover, it is not easy to apply the scheme to a self-adaptive system.

In this paper, we propose a new fully digital on-chip aging prediction circuit with a simple delay element using a 0.11 µm CMOS technology where outputs are strongly correlated with

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the $V_{th}$-degradation caused by BTI and HCI stress. The proposed circuits can be easily applied to a self-adaptive system for a reliable operation.

II. RELIABILITY PHENOMENON

As gate oxide thickness and dimension of scale shrink in integrated circuit design, reliability problems occur since nanometer transistors are stressed by high electrics field and high switching activity over extended periods of time. These stress factors lead to device aging, resulting in performance degradation and eventually design failure during the expected lifetime of the designs. The MOSFET transistor aging phenomena, such as NBTI, PBTI, HCI and TDDB, will be the most critical device degradation mechanisms and become a limiting factor in nanoscale region [15]-[17].

NBTI degradation affects PMOS transistors when a negative bias is applied to the gate or, equivalently, when the gate is grounded and a positive bias is applied to source/drain as shown in Fig. 1. The presence of hydrogenated Si-bonds (Si-H) at the interface between Si and gate oxide, boron penetration into the gate oxide, and presence of impurities in the oxide originate interface and oxide charge traps. In inversion mode, holes can be injected into these traps which lead to $V_{th}$ increase and $I_{dsat}$ decrease. An increase in $V_{th}$ reduces the voltage overdrive ($V_{DD}-V_{th}$), decreasing the circuit stability and margins. NBTI degrades performance and yield of PMOS devices. PBTI is seen for NMOS when a positive bias stress is applied across the gate oxide for the NMOS device. Although the impact of NBTI is higher than that of PBTI, PBTI has become increasingly important with the use of Hf-based dielectrics in the gate-oxide for leakage reduction [1]-[4].

HCI describes a degradation of the electrical parameters of MOSFETs under a dynamic stress mode. If a channel hot carrier collides with a crystal atom near the drain region, it may produce an electron-hole pair by impact ionization also called avalanche pair production as shown in Fig.2. Electrons from impact ionization could have enough energy to be injected into gate oxide region and charge existing oxide traps or generate new oxide-interface traps. The end result of hot carrier injection into gate oxide is a degradation of transistor parameters such as saturation current ($I_{dsat}$) and threshold voltage ($V_{th}$) [5]-[8].

TDDB is a time-dependent gate oxide breakdown when subjected to a voltage and temperature stress. The breakdown happens when a connecting path of traps is formed across the gate oxide, forming a conducting path from the gate to the substrate or gate to source and drain as shown in Fig. 3. The precise point at which the breakdown occurs is statistically distributed. As a result, only statistical averages can be predicted. For this reason, usually a large gate oxide area must be used in order to be able to detect the breakdown. Gate oxide breakdown manifests itself as an increase of gate current [9][10].

III. ON-CHIP AGING PREDICTION CIRCUIT

This section presents a new on-chip aging prediction circuit which deploys a flip-flop based delay detector for monitoring a guardband violation of sequential logics. The proposed circuit detects the moment when the critical path delay of a combinational logic in a sequential design exceeds a normal value which guarantees a correct circuit operation. That is, it monitors if the output signal transition of the combinational logic is generated at the guardband zone of the sequential design due to aging effects. The prediction circuit generates a logic “1” signal when the combinational logic brings about the guardband violation.
The core circuit for detecting the guardband violation due to aging effects consists of delay line circuit including buffer chains and a modified flip-flop for aging prediction as shown in Fig. 4. The modified flip-flop includes an exclusive-OR, a pulse generator, a two-input AND gate, and a failure decision block. In Fig. 4, all the blocks of the aging prediction circuit use a MEAS signal to turn off the prediction circuit during no-measurement mode and save power dissipation. The delay line plays an important role to delay the CLK signal, and the falling transition of the CLK signal is pushed to the guardband region. The buffer of the delay line consists of two inverters to focus on long falling transition. The Pulse_Generator makes a pulse at the falling transition time of the delayed CLK signal. The pulse width of the Pulse_Generator is dependent on the AND gate size and NMOS size.

A current output signal “D” of the combinational logic and a previous output signal “Q2” of the combinational logic is asserted to the exclusive-OR gate. When the two signals are different from each other which means the output of the combinational logic has a transition, the exclusive-OR generate logic “1”. If the logic “1” of the exclusive-OR is generated before the pre-determined guardband region, the proposed circuit makes the output a logic “1” which is generated from the AND gate with two inputs asserted from the exclusive-OR and the pulse generator. The Failure-Decision-Block makes a final output depending on the n6 signal, and it is reset every clock cycle and measurement cycle.

Figure 5 shows a timing diagram for the proposed circuit in both cases of no aging and aging failure. As shown in Fig. 5 (a), each pulse generated from the Pulse_Generator is triggered just before the guardband region. As expected, the output signal is converted to the high voltage since the input of the combinational logic has a transition, the exclusive-OR generate logic “1”. If the logic “1” of the exclusive-OR is generated before the pre-determined guardband region, the proposed circuit makes the output a logic “1” which is generated from the AND gate with two inputs asserted from the exclusive-OR and the pulse generator. The Failure-Decision-Block makes a final output depending on the n6 signal, and it is reset every clock cycle and measurement cycle.

Figure 5(a) shows the timing diagram for the proposed circuit in the case of no aging failure. As shown in Fig. 5 (a), the output signal is converted to the high voltage since the input of the combinational logic has a transition, the exclusive-OR generate logic “1”. The output signal is asserted to the AND gate with two inputs asserted from the exclusive-OR and the pulse generator. The Failure-Decision-Block makes a final output depending on the n6 signal, and it is reset every clock cycle.

Figure 5(b) shows the timing diagram for the proposed circuit in the case of aging failure. As shown in Fig. 5 (b), the output signal is converted to the high voltage after the generated pulse (or at guardband
region), so the output signal is not triggered and remains at the low voltage. In this case, an aging failure gets detected, and the output can be used as a control signal of a self-adaptive system to compensate the aging failure.

IV. EXPERIMENTAL RESULTS

The proposed circuits have been designed and evaluated using a 0.11 \( \mu \)m MOSFET technology model (VDD = 1.1V). For a long term NBTI-stress simulation, we have increased the number of cycles in the stressed input-signal with 0.5 duty cycle and 2 GHz frequency. The HCI stress time for these experiments is 400\( \mu \)sec which is not ages (run time) but actual stress time (switching time). A 4x4 multiplier has been used as a benchmark circuit in our simulation.

Table I shows that circuit level overhead associated with the proposed circuit. In the case of delay overhead, the penalty is very small because the proposed circuit does not have influence on the multiplier delay time. The power overhead in the no-measurement mode is also very small because the measurement signal is used to turn off the proposed circuit. On the other hand, in the measurement mode, the multiplier with the modified flip-flop consumes 10\% more power than that of the multiplier with a normal flip-flop. Finally, the area overhead is 28 transistors per modified flip-flop when the delay line is shared for each flip-flop. Therefore, all the simulation results show that all the overhead impact on the multiplier is very small.

<table>
<thead>
<tr>
<th>Overhead</th>
<th>Result</th>
</tr>
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<tbody>
<tr>
<td>Delay Overhead</td>
<td>&lt;1%</td>
</tr>
<tr>
<td>Power overhead (in no-measurement mode)</td>
<td>-0.1%</td>
</tr>
<tr>
<td>Power Overhead (in measurement mode)</td>
<td>-10 %</td>
</tr>
<tr>
<td>Area Overhead (Transistor count per modified F/F)</td>
<td>28 (sharing of delay elements)</td>
</tr>
</tbody>
</table>

V. CONCLUSION

This paper proposes novel on-chip aging prediction circuit in a 0.11 \( \mu \)m technology for monitoring a guardband violation of sequential logics. The simulation results show that the proposed circuits achieve a good aging failure prediction and low overhead. For a good adaptive design technique for overcoming the performance degradation due to aging phenomena, our accurate aging prediction circuit would be a practicable solution in nanoscale CMOS circuits.

REFERENCES


Kyung Ki Kim received the B.S. and M.S. degrees in electronic engineering from Yeungnam University, Kyeongsan, South Korea, in 1995 and 1997, respectively, and the Ph.D. degree in computer engineering from Northeastern University, Boston, MA, in 2008. In 2008, he was a member of the technical staff with Sun Microsystems, Santa Clara, CA, where he was involved in ROCK project. In 2009, he was a senior researcher with Illinois Institute of Technology, Chicago, IL. Currently, he is an assistant professor at Daegu University, South Korea. His current research focuses on nanoscale CMOS design, high speed low power VLSI design, analog VLSI circuit design, electronic CAD, asynchronous circuit, and nano-electronics.